

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. – 5. (Cancelled)

6. (Previously Amended) A writing method of a nonvolatile semiconductor memory device including a plurality of memory cells for storing data of 2 bits in each of said memory cells by setting four threshold voltages for each of the memory cells , comprising the steps of:

setting the four threshold voltages by changing them toward a predetermined direction starting from a first threshold voltage and sequentially setting the remaining three of the threshold voltages in order of the remotest threshold voltage from the first threshold voltage, the nearest threshold voltage to the first threshold voltage, and the second remotest threshold voltage from the first threshold voltage.

7. – 10 (Cancelled)

11. (Currently Amended) A writing apparatus for a nonvolatile semiconductor memory device including a plurality of memory cells for storing data of 2 bits in ~~one~~each of said memory ~~cell~~cells by setting four threshold voltages for each of the memory cells ~~into four thereof~~, comprising:

means for setting the four of the threshold ~~voltage~~voltages by changing them toward a predetermined direction starting from a first threshold voltage and sequentially setting the remaining three of the threshold voltages in order of the remotest threshold voltage from the first threshold voltage, the nearest threshold voltage to the first threshold voltage, and the second remotest threshold voltage from the first threshold voltage.

12. (Previously Presented) A writing apparatus for a nonvolatile semiconductor memory device according to claim 11, wherein

when setting said nearest threshold voltage to the first threshold voltage, said nearest threshold voltage to the first threshold voltage is also set to the memory cell to which the second nearest threshold voltage to the first threshold voltage is set.

13. (New) A nonvolatile semiconductor memory device, having a plurality of memory cells, for storing data of 2 bits in one memory cell by setting a threshold voltage of the memory cell to any one of four threshold voltages,

wherein each of said memory cells comprises a field effect transistor having a control gate, a floating gate, a gate insulative film, a drain area, and a source area, said field effect transistor being formed on a semiconductor substrate,

wherein the threshold voltage of the memory cell is set by changing an amount of charges which exist in the floating gate,

wherein the four threshold voltages are comprised of a first threshold voltage, a second threshold voltage, a third threshold voltage, and a fourth threshold voltage,

wherein the first threshold voltage corresponds to an erase state, the second threshold voltage is located between the first threshold voltage and the third threshold voltage, and the third threshold voltage is located between the second threshold voltage and the fourth threshold voltage,

wherein the nonvolatile semiconductor memory device executes an erase operation in which all of the memory cells, which become written targets, are set to the first threshold voltage,

wherein the nonvolatile semiconductor memory device executes a first write operation in which the memory cells, to which the fourth threshold voltage is to be set, are set to the fourth threshold voltage after the erase operation,

wherein the nonvolatile semiconductor memory device executes a second write operation in which the memory cells, to which the second threshold voltage or the third threshold voltage is to be set, are set to the second threshold voltage after the first write operation, and

wherein the nonvolatile semiconductor memory device executes a third write operation in which the memory cells, to which the third threshold voltage is to be set, are set to the third threshold voltage after the second write operation.

14. (New) A nonvolatile semiconductor memory device according to claim 13,

wherein all of the memory cells, which become written targets, are connected to the same word line, the voltage of the word line in the first write operation is higher than the voltage of the word line in the third write operation, and the voltage of the

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word line in the third write operation is higher than the voltage of the word line in the second write operation.